REMARKS

In the Office Action dated August 9, 2010, claim 5 was rejected under 35 U.S.C. § 112, ¶ 2 as being indefinite because "polysilicon layer" lacks antecedent basis. This rejection is respectfully traversed as "a polysilicon layer" is first introduced in claim 5. Withdrawal of this rejection is respectfully requested.

Further in the Office Action dated August 9, 2010, claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,126,817 to Baba et al. (hereinafter *Baba*); claims 1 and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,933,746 to Begley et al. (hereinafter *Begley*); claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable in view of U.S. Patent No. 6,791,155 to Lo et al. (hereafter *Lo*); claims 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of *Baba*; claims 2-4, 6, 7 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of *Lo* and U.S. Patent No. 6,828,646 to Marty et al. (hereinafter *Marty*); claims 2 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of *Begley* and U.S. Patent No. 6,303,464 to Gaw et al. (hereinafter *Gaw*).

With this paper, claims 2 and 9 have been canceled. Claim 1 has been amended as follows:

> performing a first fill in the form of a controlled deposition adapted to trench geometry <u>with an aspect ratio of 15 to 1 or higher</u> to thereby form oxide layers at trench walls, said oxide layers having an increasing thickness towards upper trench edges and forming a first bottleneck<u>;</u>
>
> <u>subsequently anisotropically RIE etching the oxide layers in a first step until the oxide layers-are removed from the wafer surface and subsequently continuing the RIE etching process in a second step for removing the oxide layers in an upper trench portion to a defined depth for defining a later sealing portion of the at least one void by displacing downwardly the first bottleneck to form a further bottleneck</u>.

Amended claim 1 of the present application is directed to a method of forming at least one dielectrically insulating isolation trench. The isolation trench is to reliably electrically isolate regions of different potential of device structures formed above an SOI wafer including an active semiconductor layer. Hence, it is an aspect of the present invention to use an SOI architecture.

Furthermore, according to the present invention the isolated regions shall be usable to form various device structures, such as MEMS (cf. claim 8), which require a moderately thick silicon material for the active semiconductor layer, which in turn necessitates that the isolation trenches, which have to extend down to the buried oxide layer, have a corresponding depth and, in order to not unduly consume valuable die area, thus have a high aspect ratio of 15:1 or higher. For example, for a trench width of 1 µm the depth of the trench is at least 15 µm, which is significantly greater than the depth of any trenches that are typically provided in STI (shallow trench isolation) structures, even if any such STI regions are to be provided with a comparable width.

It has been recognized by the inventors that a reliable isolation by means of such complex high aspect ratio isolation trenches can be achieved by using well-established CMOS process techniques, wherein the formation of a void by using the well-established process techniques is not to be seen as a disadvantage -- as has been the established technical opinion in the field of forming high aspect ratio isolation trenches prior to the present invention -- but on the contrary the characteristics of well established (SiO) deposition techniques may be taken advantage of in order to implement a very efficient and thus cost effective process strategy. To this end claim 1 refers to a first fill operation that is controlled so as to be adapted to the trench geometry, which in the present invention relates to an aspect ratio of 15:1 or higher.

The first fill step may be controlled such that a reliable coverage of trench sidewalls is ensured while at the same time the characteristics of well-established deposition techniques are taken into consideration, i.e., the formation of overhangs at the top of the trench, to thereby obtain the increasing thickness of the oxide layers towards the top of the high aspect ratio trench.

Since the position of the resulting bottleneck at the top of the trench is substantially independent from the trench depth, whereas the degree of narrowing depends on the process parameters that are controlled so as to reliably deposit the oxide layers on the sidewalls along the entire depth, it has been recognized by the inventors that the position of the vertical position of the bottleneck can be adjusted by a subsequent anisotropic RIE etch process, which is thus

correlated to the previous deposition step in the sense that the adapted deposition may result in a different degree of narrowing of the bottleneck, which in turn requires an appropriate "lowering" of the bottleneck so as to achieve a reliable sealing of the void at a height level that is reliably positioned below the wafer level, i.e., below a level that may be opened during further processing.

Consequently, the claimed invention provides the high aspect ratio trench for a reliable isolation and ensures an efficient process flow.

The inventive concept is neither disclosed nor suggested by the cited prior art for the following reasons.

Baba relates to an isolation trench in an SOI-type semiconductor device, wherein electrical insulation is achieved by oxidizing the exposed silicon areas. Thereafter, a polysilicon layer is deposited at high pressure (ambient pressure) so as to avoid penetration of the lower trench portions by the silicon species. This document neither discloses a controlled deposition **of oxide layers** adapted to the trench geometry, nor does this document in any way mention an adjustment, that is, lowering of a bottleneck. Hence, this document fails to teach "performing a first fill ***" and "subsequently anisotropically RIE etching ***," as recited in claim 1. Accordingly, amended claim 1 is not anticipated by *Baba*. Nor is claim 8 obvious in view of *Baba*.

Begley relates to a process in which superior fill conditions should be achieved upon filling isolation trenches having a low aspect ratio, that is, the depth is comparable to the width of the trenches. To this end, the "dogbone" structure, i.e., any overhangs at the top of the low aspect ratio trench are removed prior to conformally depositing a fill material. In addition to the fact that low aspect ratio trenches are considered in this document, the basic concept is quite different from the approach of the present invention, since a narrowing at the top of the trench is removed by a dedicated etch process, while contrary thereto, in the present invention a bottleneck is preserved by intentionally "lowering" the bottleneck or forming a bottleneck at a lower portion." Also, in those parts of this document that relate to the "prior art," a lowering or

rebuilding of a bottleneck at a lower trench portion is clearly not referred to. Hence, this document fails to teach "performing a first fill ***" and "subsequently anisotropically RIE etching ***," as recited in claim 1. Accordingly, amended claim 1 and dependent claim 11 are not anticipated by *Begley*.

Lo relates to a process strategy in which STI structures are to be formed so as to have reduced thermal stress effects during the further processing of the device. In this process, the **shallow** trench is first coated with a first dielectric layer having an increased thickness at the top of the shallow trench so as to define a constricted opening having a bottleneck structure, see column 3, lines 31-35. Thereafter, a second dielectric layer is conformally formed on the first dielectric layer, to thereby close the shallow trench and form a void therein. Thus, this document is silent with respect to providing a high aspect ratio trench, nor does this document address process flow efficiency. It appears that a conform deposition of the second dielectric layer is essential for forming the void in the shallow trench so that different deposition techniques have to be applied for forming the first and second dielectric layers, in particular when the void is to be buried deeply in the trench (cf. column 4, line 35, onwards). Hence, the concept of this document is based on a shallow trench architecture and two different deposition techniques (non-conformal and conformal) in order to form a void for stress relaxation during the further processing. This document cannot contribute to the solution, since neither SOI configurations nor high aspect ratio trenches are addressed; nor is the sequence of dedicated deposition steps in line with a highly efficient process flow based on standard CMOS processes provided.

The limitations of now cancelled claim 2 have been added to claim 1. As noted above, claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable in view of *Lo* and *Marty*.

Marty relates to a shallow trench isolation structure (cf. for instance column 5, lines 5 onward) with a trench width of 0.2 µm to 0.4 µm, in which reduced stress should be obtained. To this end, a first (conformal) dielectric material may be formed in the shallow trench and thereafter sidewall spacers are formed from the first dielectric material layer, see Fig. 3C. An etching step is then effected for defining the required profile of the spacers 7, 37, see column 5, lines 32-36. Thereafter, the deposition of the second material is performed by taking into

consideration the shape of the sidewall spacers, thereby also requiring dedicated deposition techniques correlated to the spacer etch process or at least correlated to the shape of the spacers. To this end, conformal and non-conformal deposition recipes are referred to in this document depending on the spacer shape. Furthermore, the deposition processes are to be configured so as to fill, at least partially, a trench which is believed to be wide, which additionally makes the concept non-compatible with the provision of high aspect ratio trenches. For example, depositing an oxide material so as to reliably form oxide layers with increasing thickness in very deep trenches may result in an overfill of a wide trench. Consequently, the teaching of *Marty* is quite different from the concept of the present invention, since at least the adapted deposition of the oxide layers in deep trenches is clearly not referred to, nor can this concept in any way be deduced from *Marty*. Rather, specifically selected etch processes and related deposition techniques have to applied, which cannot be transferred to SOI devices requiring high aspect isolation trenches.

The Office Action alleges that *Lo* and *Marty* are combined in order to improve the *Lo* method and to make it commercially successful. Actually, both the *Lo* and *Marty* techniques relate to stress reduction in STI regions by forming a void therein. As discussed above, *LO* follows a strategy that is based on two different deposition techniques without an intermediate etch process, wherein any excess material of the fill layers may be removed, for instance during a planarization process. Furthermore, *Lo* explicitly discloses the concept of deeply burying the void. On the other hand, the STI processing of *Marty* is based on two deposition steps, possibly in combination with a third deposition process for levelling the STI trench after the second deposition step, and an intermediate etch step possibly in combination with an additional etch step with lateral etching. Thus, it is absolutely unclear how the *Lo* process could be "improved" by implementing one or more of the features of *Marty*. It appears that the overall complexity of the process in *Marty* is greater than that of the *Lo* process. Moreover, in view of appropriately burying the void, *Lo* explicitly addresses this problem which on the other hand seems to be addressed by Marty 646 by using intermediate etch steps possibly in combination an additional third deposition step. It appears that the process technique in *Marty* specifically addresses the filling of two low aspect ratio trenches, one of which is wider and does not require a void, however requires a reliable filling. Consequently, the skilled person would clearly not combine

these techniques in view of "improving" *Lo* or make it a commercial success, as the complexity of the process would increase without any additional advantageous effect that is not already achieved by *Lo* alone.

Moreover, neither *Lo* nor *Marty* addresses reliably filling and sealing of high aspect ratio trenches by means of a first deposition step that is adapted to the high aspect ratio geometry, nor do any of these documents refer to SOI devices requiring electrically insulated device regions.

Accordingly, it is submitted *Lo* and *Marty*, whether taken singly or in combination, do not disclose or suggest the subject matter set out in claims 1, 3, 4, 6, 7 and 10.

As noted above, claims 2 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of *Begley* and *Gaw*.

Gaw US '464 relates to a method in which voids are formed in an interlayer dielectric material of a metal layer. To this end, oxide may be deposited above the metal lines and in the low aspect ratio trenches (cf. column 7, line 67), followed by a **sputter etch** process in order to reduce the thickness of the initial layer. A removal of the oxide layer in an upper trench portion is, however, not disclosed (cf. Figs 2 and 3). It appears that a removal of the oxide at the upper trench portions would indeed be rather disadvantageous since then also the metal lines would be exposed and significantly eroded during the sputter etch process. Thus, already these significant differences with respect to the etch technique and the exposure of the upper trench portions compared to the limitations added to claim 1 from now cancelled claim 2 of the present invention would not result in the solution of the present invention. Even if one were to combine *Begley* and *Gaw*, which, however, is clearly not motivated, since there is absolutely no advantage associated with implementing the etch procedure of *Gaw* in the process of *Begley* in particular as *Begley* discloses an etch process for removing the "dogbone" structure. A highly directional sputter etch process would possibly even reduce the local corner rounding effect at the top of the trench and would also result in significant etch damage at the bottom of the trench.

Accordingly, it is submitted *Begley* and *Gaw*, whether taken singly or in combination, do not disclose or suggest the subject matter set out in claims 2 and 5.

CONCLUSION

For all of the above reasons, the applicants respectfully submit that the above claims recite allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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